Synchronizing network elements on SONET/ SDH rings

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Introduction

The high-speed transport area is becoming more and more important as the need for high bandwidth increases day by day in this Information Technology oriented world. SONET / SDH technologies are becoming the backbones of most of the networks, in spite of the type of the traffic that are carried.

Unlike the Plesiochronous Digital Hierarchy (PDH) systems which uses independent, accurate clocks at switching nodes, the Synchronous Digital Hierarchy (SDH) systems follow a combination of Master-Slave and Mutual synchronization techniques. The synchronization mechanism become more complex since SDH is designed to accommodate the legacy PDH network traffic also.

This paper describes the complexity of the high-speed networks by analyzing different popular architectures and takes a look at the challenges in synchronizing various systems such as Add-Drop Multiplexers (ADM), Terminal Multiplexers, Cross Connects, line cards and other Network Elements. There are a number of standards, which are relevant in this area, and the paper concentrates on the Timing characteristics of SDH Equipment Slave Clocks (SEC). The International Telecommunication Union (ITU) recommendation for SEC timing specification is G.813. The long-term stability of the clocks, jitter and wander transfer and tolerance, the transient and holdover responses are the main specifications. Under the transient behaviour specification, there is provision for reference switching which is an inevitable feature in multiple reference systems. There are excellent PLLs available in the industry, which can satisfy the TIE (Time interval error) requirements of the specification along with the other features.

Complex Network architectures

Most of the high-speed networks engineered today are based on optical transmission through optical fibers. With the requirement for extreme reliability and availability, the networks are getting more and more complex. The systems are becoming bigger and the fault tolerance mechanisms are more prominent. Mechanisms to survive network failures are built into the architectures. The ability of a network to withstand and recover form failures is one of the most important requirements of networks. With the evolution of WDM optical networks, protection in the optical level is also being considered. With these different protection mechanisms, the synchronization architecture also becomes complex.

Two basic network failures generally considered are link and node failures. Link failure usually occurs because of physical cable cuts; node failure is due to equipment failure at network nodes. Channel failures are also possible in the optical networks, caused by the failure of transmitting or receiving equipment operating on that equipment, but from a network synchronization point of view they are not very important.

The two main techniques that have been proposed and used for protection in optical networks can be classified under two general categories, pre-designed or proactive protection and the dynamic restoration. In the pre-designed protection mechanism, protection paths are built into the system so that on the event of a failure, these paths can be used for the working traffic. But in the case of dynamic restoration, the network has to be intelligent to discover spare capacity in the network to restore the affected traffic.

Pre-designed protection schemes

In pre-designed protection, some extra resources are reserved during the system design itself, dedicated to protection purposes and kept idle when there is no failure. The efficient use of capacity is exchanged here for the efficient speed of recovery from a failure. The two main schemes currently in use are Automatic Protection Switching (APR) and Self-Healing Rings (SHR).

Automatic Protection Switching

APS is the most efficient protection scheme with point to point networks. They generally take care of the link failures. The following figures describe the different architectures with APS.

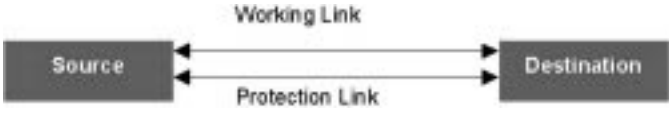


Fig.1 APS 1+1 Architecture

In 1+1 architecture, a protection link is provided for every working link, which carries traffic. The source node transmits the traffic on both the working and protection links and the

receiver at the destination node compares the two signals and chooses the better one. If one link fails, the destination node is still able to receive the signal on the operational link.

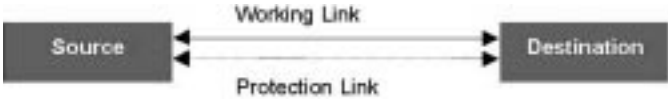


Fig.2 APS 1:1 Architecture

The 1:1 architecture is quite similar to 1+1 APS architecture, with each working link supported by a protection link, but the protection link is either idle or carry low priority traffic under normal conditions. The nodes switch the traffic to the protection link only when a failure occurs.

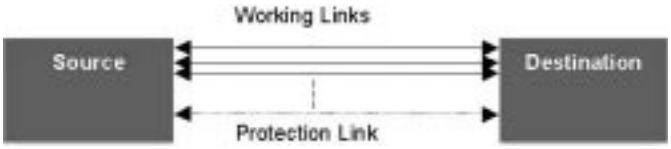


Fig 3. 1: N APS Architecture

In 1: N scheme, N working links share one protection link. It offers protection against a single failure of the N links. The link is switched back when the restoration happens and in general, an M : N protection scheme refers to an APS architecture offering protection against M failures in the N links.

Automatic Protection Switching is mainly employed in point to point network connections. It includes various Network Elements such as Terminal Multiplexers, Cross Connects, Packet routers, ATM switch interfaces. In SONET terminology, SONET NEs that have Line Termination Equipment (LTE) and terminate optical lines may provide APS.

Self Healing Rings

When the networks are designed as rings, the Self-Healing Rings mechanism is very effective, they protect from both line failures as well as node failures, since there are more than one node connected to every node.

Unidirectional SHR

The traffic goes around the ring only in one direction, and any traffic routed to the protection ring because of a traffic failure is routed in the other direction.

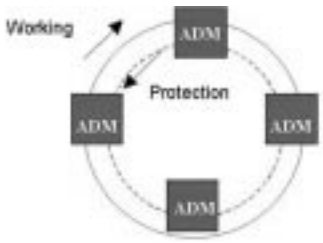


Fig 4a. USHR - L

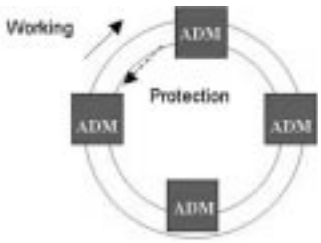


Fig 4b. USHR - P

In USHR, both line protection switching as well as path protection switching architectures are available, as shown in the figures above. The line protected USHRs basically known as USHR - L are basically has the 1:1 protection mechanism, the protection ring is idle or contains low priority traffic when there are no failures. When a particular node fails, the two adjacent nodes to the failed one loops back the traffic to the protection ring. The path protected USHR is a 1+1 protection mechanism, the working traffic is available on both the rings. Whenever a failure occurs, each node decides which signal is good and selects it.

Bi-directional Self Healing Rings

In By-directional Self-Healing Rings, (BSHR) the working traffic flows in both the rings. The basic architectures are based on two rings (BSHR - 2) and four rings (BSHR - 4).

Fig 5.a BSHR - 2

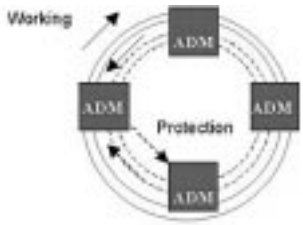


Fig 5.b BSHR - 4

The typical architectures of BSHR are two- and four-fiber line protection, namely BSHR - 2 and BSHR - 4. In BSHR -2, half of the capacity on each ring is reserved for protection. When a node failure occurs, the two nodes adjacent to the failed node redirect the affected traffic using the reserved capacity on both rings. In BSHR - 4 two fibers are dedicated as working fibers running in opposite directions, so the capacity on them can be completely utilized. Upon failure, the nodes adjacent to the failed node redirect the affected traffic from the working to the protection fibers.

Self-Healing Ring mechanisms, as the name suggests, are associated with Ring topology. The Network Elements in the ring are generally called Add-Drop Multiplexers since these devices add and extract traffic to and from the ring.

Synchronization Standards

The current generation high speed networks like SONET and SDH systems are designed for master-slave as well as mutual synchronization architecture, unlike the PDH networks where network clocks are independent and the buffers within the transceivers as well as bit stuffing mechanisms take care of the allowable frequency drift between two networks. With the SDH and SONET networks, all the clocks are traceable to a master clock, or a bunch of master clocks, the requirements for which are defined in G.811 (PRC) by the International Telecommunication Union (ITU). These are equivalent to the Stratum 1 clocks or PRS, which are defined in the North American Standards.

There are second levels of clock regenerators, which are deployed in the network, that are called the node clocks or Synchronization Supply Units, which are defined by the G.812 from ITU-T. These are equivalent to the stratum 2 clocks from the North American standard. These are also called SETS and are having the same level as the BITS clocks (Building Integrated Timing Supply). These are synchronization supply units, which provides clocks to an entire system or building and the performance of which are very close to the stratum 1 clocks. As part of SDH equipment is the SETS (Synchronization Equipment Timing Supply) Unit is defined in G.783, which describes the building blocks of SDH equipment. The clock equipment function is commonly called as the Slave Equipment Clock (SEC); equivalent to the SONET Minimum Clock (SMC) standards defined by the North American standards (Stratum 3E).

The timing flow in a Master- slave synchronized network is illustrated in the following figure.

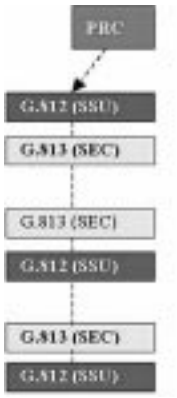


Fig 6.a ITU Synchronization plan

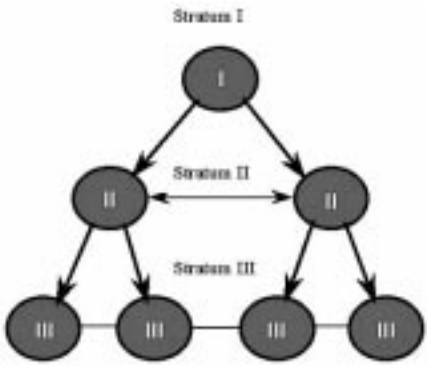


Fig 6.b North American Synchronization plan

Synchronization architectures

With the nature of complexity of the optical networks that is discussed, the synchronization becomes more complex. With the protection mechanisms built as a requirement into these systems, the performance of the synchronization mechanisms also need to be of high quality. The SONET Minimum Clock Specification and G.813 SDH Slave Equipment Clock specification detail the requirement for clocks in SDH and SONET Network Elements. Though SONET and SDH follow master-slave synchronization architecture, there are different timing modes in which the Network Element can be configured.

In External Timing mode, which is the preferred mode of synchronizing SONET NEs, a higher quality clock (G.812 or BITS wherever applicable) traceable to the PRS/PRC is used to synchronize the system. Non-traffic carrying primary rate signals are input to the timing generation unit to generate the system clocks.

In Line Timing mode, the NE has the capability to directly derive clock timing from an incoming OC-N signal and time all outgoing OC-N, OC-M, STS-1, and STS-3 signals from this clock. The primary application for this timing mode is in access rings where no BITS clock is available for external timing. There is a version of Line Timing, which is called as Loop Timing that occurs when there is only one OC-N interface. The derived OC-N clock signal is used to time the outgoing OC-N signal. This timing mode mainly applies to terminals.

When there is necessity to provide traceability from both directions to intermediate sites in UPSR ADMs applications, Through Timing is used, where each Network Element has the capability to derive clock timing from each terminating OC-N signal in each direction and pass it to outgoing OC-N in the other direction.

In Internal Timing mode, the Network Element uses its internal clock to time the outgoing OC-N/STS-1 signals. This timing mode is used in point-to-point configurations when no BITS clock is available in either office or the node is not capable of generating Hold O ver clocks.

In Holdover timing mode, the clock module is able to remember the frequency when it loose the reference, with some memory storage capability and generate the frequency locked timing.

The synchronization architecture of a ring topology is in the following figure.

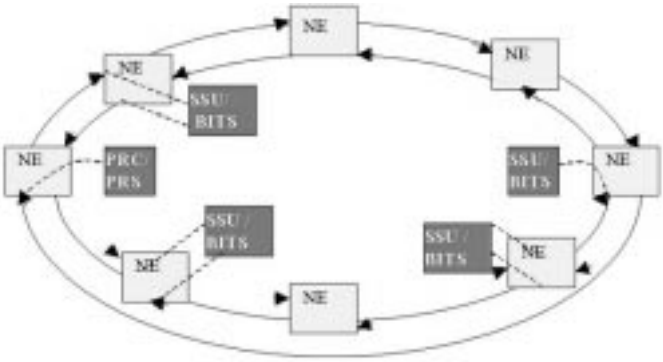


Fig. 7 SONET/SDH ring synchronization Architecture

Holdover and reference switching

A phase locked loop will be the core unit of the timing module. There are three modes of operation of these modules: normal (synchronized), holdover, and free-run. In the normal mode, the long-term average accuracy of the clock is equal to that of its synchronization source.

The holdover mode is the operating condition of a clock that has lost its controlling input and is using stored data acquired while in normal operation to control its output frequency. The accuracy of a good clock in the holdover mode starts out equal to the normal mode accuracy, and over time may slowly drift from this frequency as determined by the stability of the clock's internal oscillator.

There are noise generation, transfer and tolerance specifications on this clock module, which are the jitter and wander characteristics of the synchronization PLLs. Whenever there is a degradation in the clock the reference signal has to be isolated and a new reference has to be selected for synchronization, with out affecting the traffic in the other paths. The response to the input signal interruptions as well as reference switching of synchronization module has to follow certain specifications detailed in the standards. The synchronization module should move to a holdover mode if the input reference quality is not acceptable. Then, after checking whether the interruption in the reference is persisting, the timing module should select a new reference. Mitel Semiconductor's Digital PLL MT90401 is designed to meet all these requirements of G.813 and GR253 CORE.

Mitel's MT90401

Mitel Semiconductor's high speed PLL that performs holdover and reference switching and generates SONET/SDH clocks. The MT90401 is a digital phase locked loop (DPLL)that is designed to synchronize SDH (Synchronous Digital Hierarchy) and SONET (Synchronous Optical Network) networking equipment. The MT90401 is used to ensure that the timing of outgoing signals remains within the limits specified by Telcordia, ANSI and the ITU during normal operation and in the presence of disturbances on the incoming synchronization signals.

Applications of MT90401

Clock modules for SONET / SDH line cards

Most of the Transceivers for SDH and SONET available in the market now perform line clock extraction. The DPLL can take these derived line clocks and generate system clocks, which is compliant to G.813 and G.253CORE including the reference switching option.

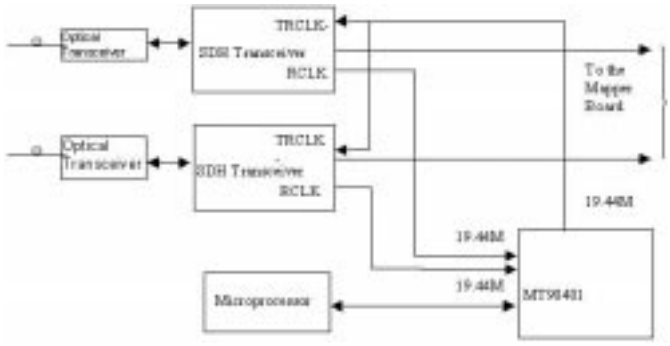
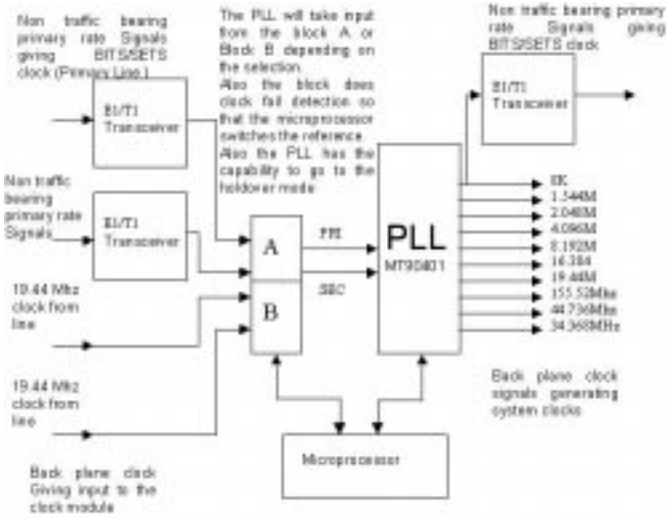


Fig 8. SDH ADM with reference switching capability

Clock Cards for SDH / SONET systems

Most of the SDH / SONET equipment deploy a separate clock card. In the following Architecture of a clock card, which takes BITS/SETS, clocks from non-traffic bearing primary rate signals as well as 19.44Mhz line clocks derived from the SDH/ SONET transceivers. There should be a multiplexing mechanism, which will select either the line-derived clocks or the BITS clocks. Also there need to be another clock fail detection logic which will monitor the clocks for fails.



Conclusion

Protection techniques in the optical networks are becoming more and more important with increasing demand for the availability of high-speed networks. By combining highly accurate network synchronization systems with advanced optical network technology, high-speed transport systems like SDH or SONET Network Elements can guarantee the high performance levels that users will demand from current and future telecommunications systems. The synchronization planning as well as performance of the synchronization systems plays a big role in the reliability and survivability of the optical networks.

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